IN THE CLAIMS

1-19. (Cancelled)

20. (Currently Amended) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a thickness equal to the second thickness of the inner leads, and wherein the peripheral part protrudes toward the second semiconductor chip and away from the first semiconductor chip.

21. (Original) An ultra-thin semiconductor package device according to claim 20, wherein the die pad is disposed below the leads.

22. (Currently Amended) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part, the peripheral part protruding towards only one of the first and second semiconductor chips;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having

a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a thickness equal to the second thickness of the inner leads, and wherein the bonding wires connected to the one of the first and second semiconductor chips are shorter than the bonding wires connected to the other semiconductor chip.

23. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein the bonding wires are connected by balls formed on the leads and stitches formed on the electrode pads.

24. (Original) An ultra-thin semiconductor package device according to claim 23, wherein metal bumps are formed on the electrode pads and wherein the stitches are formed on the metal bumps.

25. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein the die pad comprises divided first and second die pads.

26. (Original) An ultra-thin semiconductor package device according to claim 25, wherein the first and second die pads each include a corresponding chip attaching part and a corresponding peripheral part.

27. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

28. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein a thickness of the package body is about 580 μm, a thickness of the die pad peripheral part is about 100 μm, and a thickness of the chip attaching part is about 40 μm.

29. (Previously presented) An ultra-thin semiconductor package device according to claim 20, wherein an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

30. (Withdrawn) A method of manufacturing an ultra-thin semiconductor package device, said method comprising:

preparing a lead frame comprising a die pad, a tie bar connected to and supporting the die pad, and a plurality of leads disposed around the die pad;

defining a chip attaching part and a peripheral part on the die pad, said peripheral part surrounding the chip attaching part;

etching the chip attaching part so that the chip attaching part has a thickness less than a thickness of the leads;

die bonding a semiconductor chip to the chip attaching part of the die pad;

wire bonding the semiconductor chip to the leads; and

forming a package body by encapsulating the semiconductor chip, bonding wires, and a portion of the leads.

31. (Withdrawn) A method according to claim 30, wherein the thickness of the chip attaching part is between 30-50% of the thickness of the leads.

32. (Withdrawn) A method according to claim 30, wherein the die pad peripheral part and the tie bar have the same thickness as the chip attaching part.

33. (Withdrawn) A method according to claim 30, wherein the die pad peripheral part and the tie bar each have a thickness equal to the thickness of the leads.

34. (Withdrawn) A method according to claim 33, wherein the die pad peripheral part protrudes upwardly and downwardly from the chip attaching part.

35. (Withdrawn) A method according to claim 33, wherein the die pad peripheral part protrudes in a single vertical direction from the chip attaching part.

36. (Withdrawn) A method according to claim 35, wherein the die pad is disposed below the leads.

37. (Withdrawn) A method according to claim 30, wherein an upper portion of the package body has a thickness different than a thickness of a lower portion of the package body.

38. (Withdrawn) A method according to claim 30, further comprising:

preparing a wafer having a plurality of semiconductor chips formed on an active surface of the wafer;

attaching an adhesive layer to the backside of the semiconductor chips and attaching a UV tape to the adhesive layer;

irradiating the UV tape with UV light to remove the adhesiveness between the UV tape and the adhesive layer;

cutting the wafer into the plurality of semiconductor chips; and

removing the plurality of semiconductor chips from the wafer state UV tape, wherein the adhesive layer remains attached to the backside of the chips, and wherein said die bonding attaches the chips to the chip attaching part using the adhesive layer.

39. (Withdrawn) A method according to claim 30, wherein the semiconductor chip comprises a first chip attached to a top surface of the chip attaching part and a second chip attached to a bottom surface of the chip attaching part, and wherein said die bonding comprises a first die bonding step for bonding the first chip and a second die bonding step for bonding the second chip.

40. (Withdrawn) A method according to claim 30, wherein the semiconductor chip comprises a first chip attached to a top surface of the chip attaching part and a second chip attached to a bottom surface of the chip attaching part, and wherein wire bonding comprises a first wire bonding step for electrically interconnecting the first chip to the leads and a second wire bonding step for electrically interconnecting the second chip to the leads.

41. (Withdrawn) A method according to claim 30, wherein the bonding wires are connected by balls formed on surfaces of the leads and stitches formed on the electrode pads.

42. (Withdrawn) A method according to claim 35, wherein bonding wires connected to one of the chips have different lengths from the bonding wires connected to the other chip.

43. (Withdrawn) A method according to claim 36, wherein the package body has a balanced structure with reference to the semiconductor chips.

44. (Withdrawn) A method according to claim 38, wherein the wafer preparation step comprises:

attaching a UV tape to the active surface of the semiconductor chip;

grinding a backside opposite to the active surface of the semiconductor chip;

irradiating the UV tape attached to the active surface with UV light; and

removing the UV tape from the active surface of the semiconductor chip.

45. (Withdrawn) A method according to claim 30, wherein forming the package body comprises injecting a mold resin in a temperature environment ranging between about 170 and 175 °C.

46. (Withdrawn) A method according to claim 38, wherein the adhesive layer comprises an epoxy resin.

47. (Withdrawn) A method according to claim 46, wherein the adhesive layer comprises a hardener made of amine.

48. (Withdrawn) A method according to claim 46, wherein the adhesive layer comprises a coupling agent made of silane.

49. (Withdrawn) A method according to claim 30, wherein the amount of etching is determined by a pressure and an applying time of an etchant.

50. (Currently Amended) An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of single-layer leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, wherein said die pad includes a chip attaching part and a peripheral part surrounding the chip attaching part, the chip attaching part and the peripheral part having the same thickness;

a semiconductor chip having a plurality of electrode pads formed on an active surface of the chip, said chip connected to the chip attaching part;

a package body for encapsulating the semiconductor chip;

bonding wires encapsulated by the package body, said bonding wires configured to electrically connect the electrode pads of the semiconductor chip to the leads, wherein each of the plurality of single-layer leads comprises an inner lead bonded to the bonding wire and

encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body; and

wherein the chip attaching part has a first thickness and the inner lead has a second thickness that is greater than the first thickness.

51. (Original) An electronic apparatus according to claim 50, wherein the electronic apparatus is a memory card.

52-54. (Cancelled)

55. (Previously presented) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads totally having a constant second thickness greater than the first thickness, wherein the chip attaching part and the peripheral part have the same thickness.

56. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein the inner leads are formed of a single layer.

57. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein the first thickness is between about 30% to 50% of the second thickness.

58. (Previously presented) The ultra-thin semiconductor package device according to claim 55, further comprising another semiconductor chip attached to a back side of the chip attaching part.

59. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein the die pad is located below the leads.

60. (Previously presented) The ultra-thin semiconductor package according to claim 55, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

61. (Previously presented) The ultra-thin semiconductor package device according to claim 60, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

62. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

63. (Previously presented) The ultra-thin semiconductor package device according to claim 59, wherein the tie bar has the same thickness as the leads.

64. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein the tie bar has the same thickness as the die pad peripheral part.

65. (Currently Amended) The ultra-thin semiconductor package device according to claim 55, wherein the peripheral part protrudes in both vertical directions from the chip attaching part~~, and the thickness of the peripheral part is equal to the thickness of the leads~~.

66. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein the die pad comprises divided first and second die pads.

67. (Previously presented) The ultra-thin semiconductor package device according to claim 66, wherein the first and second die pads each include a chip attaching part and a peripheral part.

68. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

69. (Previously presented) The ultra-thin semiconductor package device according to claim 60, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

70. (Previously presented) The ultra-thin semiconductor package device according to claim 55, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

71. (Currently Amended) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of single-layer leads disposed around the die pad, wherein each of the plurality of single-layer leads comprises an inner lead and an outer lead, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein each of the plurality of electrode pads is electrically connected to at least one of the plurality of single-layer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and a portion of the inner leads having a second thickness greater than the first thickness, wherein the bonding wires are directly connected to the portion of the inner leads, and wherein the chip attaching part and the peripheral part have the same thickness.

72. (Cancelled)

73. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the first thickness is between about 30% to 50% of the second thickness.

74. (Previously presented) The ultra-thin semiconductor package device according to claim 71, further comprising another semiconductor chip attached to a back side of the chip attaching part.

75. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the die pad is located below the leads.

76. (Previously presented) The ultra-thin semiconductor package according to claim 71, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

77. (Previously presented) The ultra-thin semiconductor package device according to claim 76, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

78. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

79. (Previously presented) The ultra-thin semiconductor package device according to claim 75, wherein the tie bar has the same thickness as the leads.

80. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the tie bar has the same thickness as the die pad peripheral part.

81. (Cancelled)

82. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the die pad comprises divided first and second die pads.

83. (Previously presented) The ultra-thin semiconductor package device according to claim 82, wherein the first and second die pads each include a chip attaching part and a peripheral part.

84. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

85. (Previously presented) The ultra-thin semiconductor package device according to claim 76, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

86. (Previously presented) The ultra-thin semiconductor package device according to claim 71, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

87. (Currently Amended) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and tie bars connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding the chip attaching part;

a first and a second semiconductor chip each including a plurality of electrode pads connected to the leads by bonding wires, wherein the first semiconductor chip is bonded to a ~~top~~ first surface of the chip attaching part and the second semiconductor chip is bonded to a second ~~bottom~~ surface of the chip attaching part, the peripheral part protruding towards the first semiconductor chip and away from the second semiconductor chip; and

a package body encapsulating the first and the second semiconductor chips;

wherein said leads have a plurality of inner leads to which the bonding wires are bonded encapsulated within the package body, wherein said leads have a plurality of outer leads exposed from the package body, wherein the plurality of inner leads have a second thickness that is greater than the first thickness, and wherein the bonding wires connected to ~~one of~~ the first ~~and the second~~ semiconductor ~~chips~~ chip are shorter than the bonding wires connected to the ~~other one of the first and the~~ second semiconductor ~~chips~~ chip.

88. (Currently Amended) The ultra-thin semiconductor package device according to claim 87, wherein ~~the peripheral part protrudes upwards and away from the chip attaching part, and wherein the bonding wires connected to an upper one of the first and the second semiconductor chips are shorter than the bonding wires connected to a lower one of the first and the second semiconductor chips~~ the first semiconductor chip is an uppermost chip and the second semiconductor chip is a lowermost chip.

89. (Currently Amended) The ultra-thin semiconductor package device according to claim 88, wherein the ~~inner~~ plurality of leads are formed of a single layer.

90. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein the first thickness is between about 30% to 50% of the second thickness.

91. (Previously presented) The ultra-thin semiconductor package according to claim 88, wherein the bonding wires are connected to the leads by balls formed on the surface of the leads and wherein the bonding wires are connected to the electrode pads by stitches formed on the electrode pads.

92. (Previously presented) The ultra-thin semiconductor package device according to claim 91, wherein a metal bump is formed on the electrode pads and the stitches are formed on the metal bumps.

93. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

94. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein the tie bars have the same thickness as the leads.

95. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein the tie bars have the same thickness as the peripheral part.

96. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the second thickness.

97. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein the die pad comprises divided first and second die pads.

98. (Previously presented) The ultra-thin semiconductor package device according to claim 97, wherein the first and second die pads each include a chip attaching part and a peripheral part.

99. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein an adhesive bonds the first and the second semiconductor chips to the chip attaching part.

100. (Previously presented) The ultra-thin semiconductor package device according to claim 99, wherein the first and the second semiconductor chips are memory devices and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

101. (Previously presented) The ultra-thin semiconductor package device according to claim 88, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

102. (Previously presented) The ultra-thin semiconductor package device according to claim 87, wherein the peripheral part protrudes downwards and away from the chip attaching part, and wherein the bonding wires connected to a lower one of the first and the second semiconductor chips are shorter than the bonding wires connected to an upper one of the first and the second semiconductor chips.

103. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein the inner leads are formed of a single layer.

104. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein the first thickness is between about 30% to 50% of the second thickness.

105. (Previously presented) The ultra-thin semiconductor package according to claim 102, wherein the bonding wires are connected to the leads by balls formed on the surface of the leads and wherein the bonding wires are connected to the electrode pads by stitches formed on the electrode pads.

106. (Previously presented) The ultra-thin semiconductor package device according to claim 105, wherein a metal bump is formed on the electrode pads and the stitches are formed on the metal bumps.

107. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

108. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein the tie bars have the same thickness as the leads.

109. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein the tie bars have the same thickness as the peripheral part.

110. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the second thickness.

111. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein the die pad comprises divided first and second die pads.

112. (Previously presented) The ultra-thin semiconductor package device according to claim 111, wherein the first and second die pads each include a chip attaching part and a peripheral part.

113. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein an adhesive bonds the first and the second semiconductor chips to the chip attaching part.

114. (Previously presented) The ultra-thin semiconductor package device according to claim 113, wherein the first and the second semiconductor chips are memory devices and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

115. (Previously presented) The ultra-thin semiconductor package device according to claim 102, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

116. (Currently Amended) An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a first semiconductor chip mounted to ~~the die pad~~ a first side of the chip attaching part and ~~another~~ a second semiconductor chip mounted to ~~another~~ a second side of the chip attaching part, said first and second semiconductor ~~chip~~ chips having a plurality of electrode pads, the peripheral part protruding towards the first semiconductor chip and away from the second semiconductor chip, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a second thickness greater than the first thickness.

117. (Cancelled)

118. (Previously presented) The semiconductor package device of claim 50, wherein the first thickness is between about 30% to 50% of the second thickness.

119. (Cancelled)

120. (Previously presented) The semiconductor package device of claim 50 further comprising another semiconductor chip attached to a back side of the chip attaching part.

121. (Previously presented) The semiconductor package device of claim 50, wherein the die pad is located below the leads.

122. (Previously presented) The semiconductor package of claim 50, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

123. (Previously presented) The semiconductor package device of claim 122, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

124. (Previously presented) The semiconductor package device of claim 50, wherein an upper portion of the package body above the leads and a lower portion of the package body below the leads have different thicknesses.

125. (Previously presented) The semiconductor package device of claim 121, wherein the tie bar has the same thickness as the leads.

126. (Previously presented) The semiconductor package device of claim 50, wherein the tie bar has the same thickness as the die pad peripheral part.

127. (Cancelled)

128. (Previously presented) The semiconductor package device of claim 50, wherein the die pad comprises divided first and second die pads.

129. (Previously presented) The semiconductor package of claim 128, wherein the first and second die pads each include a chip attaching part and a peripheral part.

130. (Previously presented) The semiconductor package device of claim 50, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

131. (Previously presented) The semiconductor package device of claim 122, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

132. (Previously presented) The semiconductor package device of claim 50, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

133. (Previously presented) The ultra-thin semiconductor package device of claim 58, wherein the semiconductor chip and the another semiconductor chip are of the same type.

134. (Previously presented) The ultra-thin semiconductor package device of claim 74, wherein the semiconductor chip and the another semiconductor chip are of the same type.

135. (Previously presented) The ultra-thin semiconductor package device of claim 116, wherein the peripheral part protrudes from only one side of the chip attaching part.

136. (Previously presented) The ultra-thin semiconductor package device of claim 116, wherein the peripheral part protrudes upward from the chip attaching part.

137. (Previously Presented) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

at least one semiconductor chip, the at least one semiconductor chip including a plurality of electrode pads, wherein the at least one semiconductor chip is bonded to a surface of the chip attaching part;

a package body encapsulating the at least one semiconductor chip; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads have a second thickness, wherein the first thickness is smaller than the second thickness, and wherein the peripheral part only protrudes downward.

138. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a top surface of the chip attaching part.

139. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a bottom surface of the chip attaching part.

140. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the at least one semiconductor chip is attached to a top surface of the chip attaching

part, and wherein at least one other semiconductor chip is attached to a bottom surface of the chip attaching part.

141. (Previously presented) The ultra-thin semiconductor package device of claim 137, wherein the peripheral part has a thickness equal to the second thickness.

142. (New) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

a semiconductor chip, the semiconductor chip including a plurality of electrode pads, the semiconductor chip bonded to a surface of the chip attaching part, the peripheral part only protruding away from the semiconductor chip;

a package body encapsulating the semiconductor chip; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, the inner leads having a second thickness that is greater than the first thickness.